PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Edoardo BOTTI et al.
Serial No.: 09/943,414
Confirmation No.: 7795
Filed: August 30, 2001
For: ADJUSTABLE HARMONIC DISTORTION DETECTOR AND METHOD FOR USING THE SAME

: Atty. Docket No.: 00-CA-135/GC
: Group Art Unit: 2816

CLAIM FOR PRIORITY UNDER 35 USC §119

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Under the provisions of 35 USC §119, there is filed herewith a certified copy of European Application No. 00-830596.3, filed September 1, 2000, in accordance with the International Convention for the Protection of Industrial Property, 53 Stat. 1748, under which Applicants hereby claim priority.

Respectfully submitted,

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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

00830596.3

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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.: 00830596.3
Demande n°:

Anmeldetag:
Date of filing: 01/09/00
Date de dépôt:

Anmelder:
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Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
Adjustable harmonic distortion detector, and method using same detector

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

Staat: State: Pays:	Tag: Date: Date:	Aktenzeichen: File no. Numéro de dépôt:

Internationale Patentklassifikation:
International Patent classification:
Classification internationale des brevets:
G01R23/20

Am Anmeldetag benannte Vertragstaaten:
Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/TR
Etats contractants désignés lors du depôt:

Bemerkungen:
Remarks:
Remarques:

"Adjustable harmonic distortion detector, and method using same detector".

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DESCRIPTION

The present invention relates to an adjustable harmonic distortion detector, and method using same detector, particularly for linear (AB class) and switching (D class) amplifiers.

The term distortion designates any undesired deformation in the time trend of a signal and we distinguish two types of distortion; a) linear; b) non linear.

The linear distortion happens when an input sinusoidal signal having a given amplitude and a given phase causes a still sinusoidal output signal having a different amplitude and/or phase.

The non linear distortion happens when an input sinusoidal signal causes an output signal which is no longer as such.

Particularly, in this last case, the distortion is measured in function of the deformation that the sinusoidal signal suffers, being founded on the possibility of dividing said deformed signal, into a sinusoidal oscillation having the same frequency (called fundamental oscillation) and into a number "n", with "n" rising to infinity, of oscillations having multiple frequencies of the fundamental (called harmonic oscillations).

We assume as convention, as a measure of the total harmonic distortion T.H.D., the ratio, usually expressed per cent, between the total efficacious value of the harmonics and the efficacious value of the fundamental.

The distortion entity has a particular importance in the acoustic frequency amplifiers, that is for audio amplifiers, because it can modify the signal intelligibility.

An usual function in said audio amplifiers is the so called distortion detector function, called "clipping function", that has the role to detect when an amplifier has reached the peak power.

Using this information we can limit the distortions that a signal outgoing from the amplifier suffers, distortions due to the reached threshold of saturation of the same amplifier.

In this way by means of opportune circuits we can define "a priori" a fixed level of acceptable distortion, that is we can define at which distortion level the clipping function can interfere so as to reduce the amplifier gain, limiting, therefore, the distortion inside desiderated ranges.

The circuits now used are essentially of three categories: a) by a sensor of the saturation of the output power transistor of the audio amplifier, able to detect a distortion at a prefixed threshold value, as shown in Figure 1 wherein we note an ideal output signal 1, a distorted signal 2 and a prefixed intervention threshold 3; b) by a comparison between the peak voltage of the input signal and the peak voltage of the same signal at the output of the audio amplifier when this last output signal is distorted, as shown in Figure 2; c) by a measurement of the unbalance of the input pins of the audio amplifier (in fact during the normal working the input pins are at the same voltage, while when the amplifier saturates the pins assume a voltage difference that depends on the input signal amplitude).

The circuits heretofore described work correctly only in the case of AB class amplifiers, give troubles if the amplifier is D class and mostly if the amplifier is implemented in an integrated circuit wherein the output signal is not available inside the same integrated circuit.

In view of the state of the art described, it is an object of the present invention to realize a circuit able to work both with linear and non linear amplifiers.

Moreover an object of the present invention is to realize a circuit able to detect the reaching of the total harmonic distortion at the output of an amplifier.

According to the present invention, such objects are achieved by an adjustable harmonic distortion detector comprising a clock signal source,

means for the detection of a first period of evaluation and means for the detection of a second period of evaluation, characterized in that a first block memorizes a number equal to the clock pulses present in said first period of evaluation, a multiplier block makes a multiplication between said number stored in said first block and a multiplicative factor during said second period of evaluation, a second block memorizes the result of said multiplication, said second block adapted to generate an output signal when said result in said second block is equal to zero.

Moreover such objects are achieved by an adjustable harmonic distortion detector comprising a clock signal source and frequency multiplier/divider means, means for the detection of a first period of evaluation and means for the detection of a second period of evaluation, characterized in that a first block memorizes a number equal to the clock pulses present in said first period of evaluation, said frequency multiplier/divider means generate a modified clock signal, a third block counts the clock pulses present in said modified clock signal, a comparator compares said number stored in said first block with the number stored in said third block, said comparator adapted to generate an output signal when said comparison is equal to zero.

Moreover such object is achieved by a method to detect the harmonic distortion, characterized by computing the length of a first period of evaluation, computing the length of a second period of evaluation, receiving in input a prefixed value of total harmonic distortion so to generate an output signal showing the reaching of the value of the prefixed distortion.

Moreover such objects are achieved by a method to detect the harmonic distortion, characterized by comprising the following steps:

a) to count the number of clock signal pulses in a first period of evaluation;

b) to insert said number in a first block;

c) to insert a multiplicative factor in a second block;

d) to multiply the value stored in said first block for the value stored in second block during a second period of evaluation;

e) to decrease the outcome of the step (d) during second period of evaluation;

f) to generate a signal in the case of the outcome of the step (e) is zero.

Moreover such object is achieved by a method to detect an harmonic distortion, characterized by comprising the following steps:

a) to count the number of clock signal pulses in a first period of evaluation;

b) to insert said number into a third block;

c) to modify said clock signal into a modified clock signal;

d) to count the number of modified clock signal pulses present in a second period of evaluation;

e) to insert the outcome of the step (d) in a fourth block;

f) to compare the outcomes of the steps (b) and (e) during second period of evaluation;

g) to generate an output signal in the case the outcome of the phase (f) is equal to zero.

Thanks to the present invention it is possible to realize a circuit able to work both with AB class linear audio amplifiers and with D class audio amplifiers.

Moreover it is possible to realize a circuit that controls the distortion of the output signal in function of the frequency of the same signal.

Moreover it is possible to realize a completely integrated circuit, without the use of external capacities.

The features and the advantages of the present invention will be made evident by the following detailed description of an embodiment thereof which is illustrated as not limiting example in the annexed drawings, wherein:

Figure 1 shows a voltage/time graph of a signal outgoing from an audio amplifier according to the prior art;

Figure 2 shows another voltage/time graph of a signal outgoing from an audio amplifier according to the prior art;

Figure 3 shows another voltage/time graph of a signal outgoing from an audio amplifier according to the prior art;

Figure 4 shows a voltage/time graph of a clipping signal according to the prior art;

Figure 5 shows a diagram according to the present invention;

Figure 6 shows a first embodiment of the circuit according to the present invention;

Figure 7 shows a second embodiment of the circuit according to the present invention;

Figure 8 shows a third embodiment of the circuit according to the present invention;

Figure 9 shows a fourth embodiment of the circuit according to the present invention.

In Figure 3 a graph 5 having an abscissa axis indicating the time and an ordinate axis indicating the voltage, is shown. The graph 5 is formed by an output signal 7 that shows the output signal of an amplifier in the ideal case, that is in the case in which there aren't distortions, and by a distorted signal 6 due to the saturation of the amplifier.

We can identify, particularly, two time periods: 1) T1 adapted to provide the period length from the crossing of the abscissa axis to the start of the clipping phase, also called zero-crossing period; 2) T2 adapted to provide the period length from the start of the clipping phase to the end of the same, also called clipping period.

The period T2 establishes, as we can deduce from the Figure 4, also the period of a square wave signal, also called detected clipping signal.

This signal is able to provide information on the distortion of the

output signal 6 from the amplifier.

By a numerical simulation the Applicant has found that a correlation exists between the ratio of the clipping period length (T2) and the zero-crossing period length (T1) with the percent of the total harmonic distortion (T.H.D.). Moreover the Applicant has found that the correlation between (T2/T1) and T.H.D. is independent from the frequency of the distorted output signal 6 from the audio amplifier. Finally the Applicant has plotted said ratio (T2/T1) versus said distortion T.H.D. by means of a diagram, as shown in Figure 5.

In the diagram of Figure 5 we note an abscissa axis indicating the T.H.D., expressed in percent, and an ordinate axis indicating the dimensionless ratio T2/T1. We note also a curve 8 that has a trend which grows with the growth of the percent value of T.H.D.

The utility of such a diagram will be evident hereinafter in the description of the embodiments of the invention.

In Figure 6 a first embodiment of the circuit according to the invention is shown.

In this Figure we note a clock signal 9 obtained from a local clock source (not shown in Figure), a zero-crossing signal 10 or period T1, deduced by crossing detector means for the abscissa axis of an input analog signal (not shown in Figure) and a clipping signal 11 or period T2, deduced by detector means known to a skilled person.

The zero-crossing signal 10 by through a reset/enable pin 14 sets to zero the content of a block 12 of increment type, also called up counter, and determines the start of the counting of the clock signal 9 through a data input pin 13.

The block 12, therefore, starts to count from zero the clock signal pulses with a counting rate equal to said clock frequency. The block 12 stores the pulse numbers included in every output signal which crosses the abscissa axis, both in the case of positive and negative half-wave.

In this way the block 12 contains a number indicative of the rapidity of the distorted output signal 6 from the audio amplifier during the evaluation period T1.

The output 21 of the block 12, during the period T2, sets the number of clock pulses of the signal 9, counted in the period T1, in a first register 15 of a multiplier block 16.

In a block 18, a user has previously stored a numeric value that represents the harmonic distortion level that we want as top threshold. This value is deduced from the diagram shown in Figure 5.

Said block 18 can be implemented, for example, as a R.O.M. device (Red Only Memory).

For example, if we want to have a T.H.D. equal to 5%, that is a total harmonic distortion of the signal equal to 5%, a value equal to 0.9 must be present in the block 18, as we deduce from the diagram of Figure 5.

The multiplier block 16, therefore, makes a multiplication operation between what is stored in the first register 15 and what is stored in a second register 19. In said second register there is the number chosen by the user and stored in the block 18, that is in said second register there is a multiplicative factor by means of which it is possible to establish the correlation between the ratio T2/T1 and T.H.D.

In order that the block 16 makes said operation of multiplication the signal clock 9 and the clipping signal 11 must provide simultaneously the qualification, by, respectively, a pair of enable pins 20 and 17.

The output 22 of the block 16 is then loaded in a block 23 of decreasing type, also called down counter, by means of a data input pin 24.

Said block 23 decreases, with a decreasing rate equal to the frequency of said clock signal 9, the output 22 received in input for all the time during which the clipping signal 11 is turned on, that is for all the length of the period T2.

The qualification to the decreasing operation of the computed value by

the block 16, is obtained by means of the simultaneously combination of the clock signal 9 and the clipping signal 11, by, respectively, a pair of pin 25 and 26.

When the value stored in said block 23 reaches the zero, the output 27 is activated giving the information of the reaching of the fixed T.H.D.

During the period T2, in the case the value stored in the block 23 does not reach the zero or the clipping signal 11 is not turned on, the block 23 does not generate any signal.

If the output signal 27 is high and the period T2 is not completely elapsed, said output signal 27 remains high until the period T2 is elapsed.

The invention, in this particular embodiment, therefore consists in counting how many clock pulses are present in the distorted output signal 6 during the period T1, multiplying said value for a number, known a priori, deduced from the experimental diagram of Figure 5 and finally generating an output signal 27 in the case of the block 23 reaches the zero inside the period T2, so to generate said output distortion detector signal 27.

Therefore the down counter 23 generates the signal 27 when the input signal 22 has reached the fixed value T.H.D. or the equivalent ratio T2/T1 deduced from the diagram of Figure 5.

In the case we want a detection of the distortion in function of the frequency of the distorted output signal 6 of the amplifier, that is, in the case we want to detect the distortion not as a fixed value but as a value variable in function of the rapidity of the front of the signal, the circuit previously shown must be modified as that shown in Figure 7.

In Figure 7,besides elements already described in Figure 6, a block 28 having an input signal 29, that represents the number of clock pulses stored by the block 12, and an output signal 30, that represents the value being in said second register 19 of said multiplier block 16, is shown.

The block 28 makes a correspondence function between the number of the clock pulses counted during the measure period of the block 12, that is

during the period T1, and the diagram shown in Figure 5.

Said block 28, therefore, realizes a reference table between the number of counted clock pulses during T1 and the diagram of Figure 5.

The block 28 can be implemented by a R.O.M. type device or by a microprocessor.

The block 28 defines a table so that a determined value of the ratio T2/T1 corresponds to every particular number of counted clock pulses, so as to detect how much the front side of the sinusoidal signal outgoing from the amplifier is steep.

For example, a possible table can be as:

Num. Of Clock Pulses	T2/T1 or T.H.D.
0-10	0.4
11-100	1
101-1000	1.2

In this way we obtain a multiplicative factor which is a function of the number of the counted clock pulses.

The invention, in this particular embodiment, therefore consists in counting how many clock pulses are present in the distorted output signal 6 during the period T1, multiplying said value for a number which is a function of said counting and is deduced from the experimental diagram of Figure 5 and finally generating said output signal 27 in the case of the block 23 reaches the zero inside the period T2, so to generate said output distortion detector signal 27 in function of the frequency of the output distorted signal 6.

In the case during the period T2, the value stored in the block 23 does not reach the zero or the clipping signal 11 is not turned on, the block 23 does not generate any signal.

If the output signal 27 is high and the period T2 is not completely passed, said output signal 27 remains high until the period T2 is passed.

In Figure 8 another embodiment of the circuit according to the present invention is shown.

As shown in this Figure, besides elements already described in Figures 6 and 7, we note that the clock signal 9 is counted by the block 12, during the period T1, as described previously in Figure 6, and that said clock signal 9 is also the input of a block 31.

Said block 31 generates an output clock signal 32 modified in frequency, that is said block 31 acts as a frequency multiplier or divider.

For example the clock signal 32 is equal to 3/2 of the clock signal 9 so as to obtain a ratio T2/T1 equal to 0.4.

Said modified clock signal 32 is counted by another block 39 of up counter type during the period T2. In fact the block 39 receives in input said signal 32, by means of a reset/enable pin 50, and starts the counting of the clock pulses from zero, by means of a data input pin 40.

The outcomes stored in said blocks 12 and 39 are set on the respective outputs 21 and 33 that act as input signals for a block 34, by means of respective input pins 37 and 36.

The block 34 has also in input, by means of the pin 35, said clipping signal 11.

The block 34 compares the input signals 21 and 33 during the period T2 and it generates an output signal 38 when said output signals 21 and 33 have an equal value.

Therefore the comparator block 34 sets on the output 38 the detector pulse, function of the ratio between the frequency values of the clock signal 9 and of the modified clock signal 32.

The circuit shown in Figure 8 is convenient in those cases wherein the T.H.D. does not change continuously , that is a circuit particularly suitable for those cases in which we have some fixed points for the intervention T.H.D. threshold.

Moreover it also advantageous with respect to the circuit shown in

Figure 7 because it does not foresee the use of a multiplier block 16 but it foresees the use of a comparator block 34 of simplified construction.

For example in this particular embodiment we have that the ratio T2/T1 is given by the frequency ratio of the clock signal 9 and the modified clock signal 32.

If the frequency of the clock signal 9 is equal to the frequency of the modified clock signal 32, then the circuit detects a T.H.D. equal to the 6% because T1/T2 = 1. We deduce from the diagram of Figure 5 the T.H.D. value equal to 6%.

The invention, in this particular embodiment, therefore consists in counting how many clock pulses are present in the distorted output signal 6 during the period T1, and counting how many pulses of modified clock signal pulses 32 are present during the period T2, comparing said counts by means of the comparator block 34 until they are both equal to zero during the period T2, so as to generate an output distortion detector signal 38.

Therefore the comparator 34 generates the signal 38 when the input signals 21 and 33 reach the prefixed value T.H.D. or the equivalent ratio T2/T1 deduced from the diagram of Figure 5.

During the period T2, in the case the value stored in the block 34 does not reach the zero or the clipping signal 11 is not turned on, the block 34 does not generate any signal.

If the output signal 38 is high and the period T2 is not completely elapsed, said output signal 38 remains high until the period T2 is elapsed.

In Figure 9 another embodiment of the circuit of Figure 8 is shown and particularly there is a block 41 that receives in input the signal 21 that represents the counting made by the block 12 during the period T1.

Said block 41 is a reference table between the number of counted clock pulses during the measure period of the block 12 and the diagram shown in Figure 5.

For example, a possible table can be as:

Num. Of Clock Pulses	T2/T1 or T.H.D.
0-10	0.4
11-100	1
101-1000	1.2

The block 41 is implemented as a R.O.M. device or as a microprocessor device.

The block 41 generates an output signal 42 that is set in input to the block 31, by means of a data input pin 44. The block 31 itself generates a modified clock signal 43 so to that said signal 43 is a function of the length of the period T1.

The signal 43 is set in input to the block 39 of up counter type, by means of a data input pin 40, and it is enabled to the counting by the clipping signal 11, by means of the erase/enable pin 50.

Said block 39 generates an output signal 47 that is set in input to said comparator block 34 so that the comparison between said signal 47 and said signal 21 is made.

The block 41, as previously described in Figure 7, gives to every number of counted clock pulses a value deduced from the diagram of Figure 5 and said value serves to the block 31 to decide how to change the clock signal 9.

Therefore the comparator block 34 sets on the output 38 the detector pulse, in function of the ratio between the frequency values of the clock signal 9 and of the modified clock signal 32.

The circuit shown in Figure 9 is convenient in those cases in which the T.H.D. changes continuously, that is it is a circuit particularly suitable for those cases in which we have a curve as reference for the T.H.D. threshold of intervention.

The invention, in this particular embodiment, therefore consists in counting how many clock pulses are present in the distorted output signal 6 during the period T1, and counting how many pulses of modified clock

signal 42, function of the counting of the clock signal 9 during the period T1, are present during the period T2, comparing said counts by means of the comparator block 34 until they are equal to zero during the period T2, so as to generate an output distortion detector signal 38, in function of the frequency of said distorted output signal 6.

During the period T2, in the case of the value stored in the block 34 does not reach the zero or the clipping signal 11 is not turned on, the block 34 does not generate any signal.

If the output signal 38 is high and the period T2 is not completely elapsed, said output signal 38 remains high until the period T2 is elapsed.

By means of simple combinatory circuits, a possible embodiment of which is not shown because they are prior art, we can also determine the length of the pulse of the T.H.D. value at multiplies of the frequency of the signal clock or we can cause said pulse to start at the reaching of the value of T.H.D., and the T.H.D. signal to remain high until the period T2 is elapsed.

CLAIMS

1. An adjustable harmonic distortion detector comprising a clock signal source (9), means for the detection of a first period of evaluation (T1) and means for the detection of a second period of evaluation (T2), characterized in that a first block (12) memorizes a number equal to the clock pulses present in said first period of evaluation (T1), a multiplier block (16) makes a multiplication between said number stored in said first block (T1) and a multiplicative factor during said second period of evaluation (T2), a second block (23) memorizes the outcome of said multiplication, said second block (23) adapted to generate an output signal (27) when said outcome in said second block (23) is equal to zero.

2. An adjustable harmonic distortion detector comprising a clock signal source (9) and frequency multiplier/divider means (31), means for the detection of a first period of evaluation (T1) and means for the detection of a second period of evaluation (T2), characterized in that a first block (12) memorizes a number equal to the clock pulses present in said first period of evaluation (T1), said frequency multiplier/divider means (31) generate a modified clock signal (43), a third block (39) counts the clock pulses present in said modified clock signal (43), a comparator (34) compares said number stored in said first block (12) with the number stored in said third block (39), said comparator (34) adapted to generate an output signal (38) when said number in said first block (12) and said number in said third block (39) are equal to zero.

3. Distortion detector according to the claim 1, characterized in that said multiplicative factor is a fixed number known a priori.

4. Distortion detector according to the claim 1, characterized in that said multiplicative factor is function of the number of the clock signal pulses (9) stored in said first block (12).

5. Distortion detector according to the claim 2, characterized in that said frequency multiplier/divider means (31) make a multiplication/division for a

fixed number known a priori.

6. Distortion detector according to the claim 2, characterized in that said frequency multiplier/divider means (31) make a multiplication/division for a number function of the value stored in said first block (12).

7. Distortion detector according to the claim 1, characterized in that said multiplicative factor is deduced from the correlation between the ratio of said second (T2) and first (T1) period of evaluation and the total distortion value (T.H.D.) according with a diagram (8).

8. Distortion detector according to the claim 1, characterized in that said first block (12) receives in input said clock signal (9), said first evaluation period (T1), and that said multiplier block (16) receives in input said cloak signal (9), said multiplicative factor and the output signal (21) of said first block (12), and that said second block (23) receives in input said clock signal (9), the output signal of said multiplier block (16), said second evaluation period (T2) and produces an output signal (27) during the simultaneously combination of said clock signal (9) and of said second evaluation period (T2).

9. Distortion detector according to the claim 1, characterized in that said first block (12) receives in input said clock signal (9), said first evaluation period (T1), and that said multiplier block (16) receives in input said clock signal (9), said second evaluation period (T2) and a signal (30) generated by a fourth block (28) adapted to realize a correspondence function between the number of clock pulses counted in the measure period (T1) of said first block (12) and said diagram (8), and that said second block (23) receives in input said clock signal (9), the output signal of the multiplier block (16), said second evaluation period (T2) and it produces an output signal (38) during said second evaluation period (T2).

10. Distortion detector according to the claim 2, characterized in that said first block (12) receives in input said clock signal (9), said first evaluation period (T1), and that said frequency multiplier/divider means (31)

receive in input said clock signal (9), that said third block (39) receives in input the output (32) of said frequency multiplier/divider means (31), said second evaluation period (T2), and that said comparator receives in input the output signal of said first block (12), the output signal of said third block (39) and said second evaluation period (T2) and it produces an output signal (38) during said second evaluation period (T2).

11. Distortion detector according to the claim 2, characterized in that said first block (12) receives in input said clock signal (9), said first evaluation period (T1), and that said frequency multiplier/divider means (31) receive in input said clock signal (9), said first evaluation period (T1), and an output signal (42) of a fifth block (41), and that said third block (39) receives in input the output (32) of said frequency multiplier/divider means (31), said second evaluation period (T2), and that said comparator receives in input the output signal of said first block (12), the output signal of said third block (39) and said second evaluation period (T2) and it produces an output signal (38) during said second evaluation period (T2).

12. Method to detect the harmonic distortion, characterized by computing the length of a first period of evaluation (T1), computing the length of a second period of evaluation (T2), receiving in input a prefixed value of total harmonic distortion so as to generate an output signal (27, 38) showing the reaching of the value of the prefixed distortion.

13. Method to detect the harmonic distortion, characterized by comprising the following steps:

a) to count the number of clock signal pulses (9) in a first period of evaluation (T1);

b) to insert said number in a first block (12);

c) to insert a multiplicative factor in a second block; (18)

d) to multiply the value stored in said first block (12) for the value stored in said second block (18) during a second period of evaluation (T2);

e) to decrease the outcome of the step (d) during said second period

of evaluation (T2);

f) to generate a signal (27) in the case that the outcome of the step (e) is zero.

14. Method to detect an harmonic distortion, characterized by comprising the following steps:

a) to count the number of clock signal pulses (9) in a first period of evaluation (T1);

b) to insert said number in a first block (12);

c) to modify said clock signal (9) in a modified clock signal (32);

d) to count the number of modified clock signal pulses (32) present in a second period of evaluation (T2);

e) to insert said outcome of the step (d) in a third block (39);

f) to compare the outcomes of the steps (b) and (e) during second period of evaluation (T2);

g) to generate an output signal (38) in the case the outcome of the step (f) is equal to zero.

15. Method according to the claim 13, characterized in that said multiplicative factor is a fixed number known a priori.

16. Method according to the claim 13, characterized in that said multiplicative factor is a value (30) in function of the pulse number stored in said first block (12).

17. Method according to the claim 14, characterized in that said modified clock signal (43) is deduced by multiplication/division for a fixed number known a priori.

18. Method according to the claim 14, characterized in that said modified clock signal (43) is deduced by multiplication/division for a number (42) which is a function of the value present in said first block (12).

19. Distortion detector according to anyone of previous claims, characterized in that said first evaluation period (T1) provides the length from the crossing of the abscissa axis to the start of the distortion step of

said output signals (7).

20. Distortion detector according to anyone of previous claims, characterized in that said second evaluation period (T2) provides the length from the start of the distortion step to the end of the same of said output signals (27, 38).

21. Distortion detector according to anyone of previous claims, characterized in that said first block (12) and said third block (39) are up counters.

22. Distortion detector according to anyone of previous claims, characterized in that said second block (23) is a down counter.

23. Distortion detector according to any previous claims, characterized in that said fourth block (41) makes the correspondence function between the number of clock pulses counted in said first evaluation period (T1) and stored in said first block (12) and said diagram (8).

"Adjustable harmonic distortion detector, and method using same detector".

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ABSTRACT

The present invention relates to an adjustable harmonic distortion detector comprising a clock signal source (9), means for the detection of a first period of evaluation (T1) and means for the detection of a second period of evaluation (T2). Said detector has the characteristic that a first block (12) memorizes a number equal to the clock pulses present in said first period of evaluation (T1), a multiplier block (16) makes a multiplication between said number stored in said first block (T1) and a multiplicative factor during said second period of evaluation (T2), a second block (23) memorizes the outcome, said second block (23) adapted to generate an output signal (27) when said outcome in said second block (23) is equal to zero. (Figure 6).

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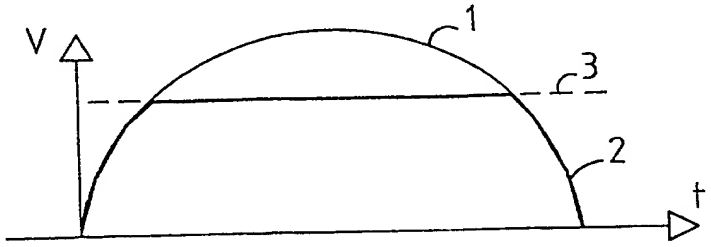

Fig.1

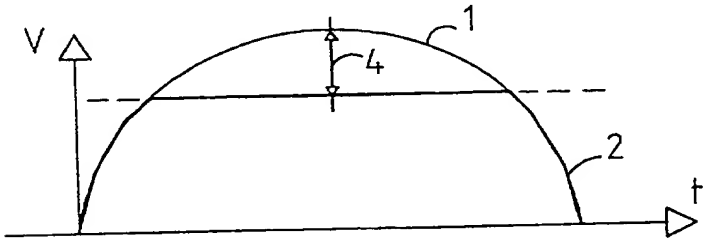

Fig.2

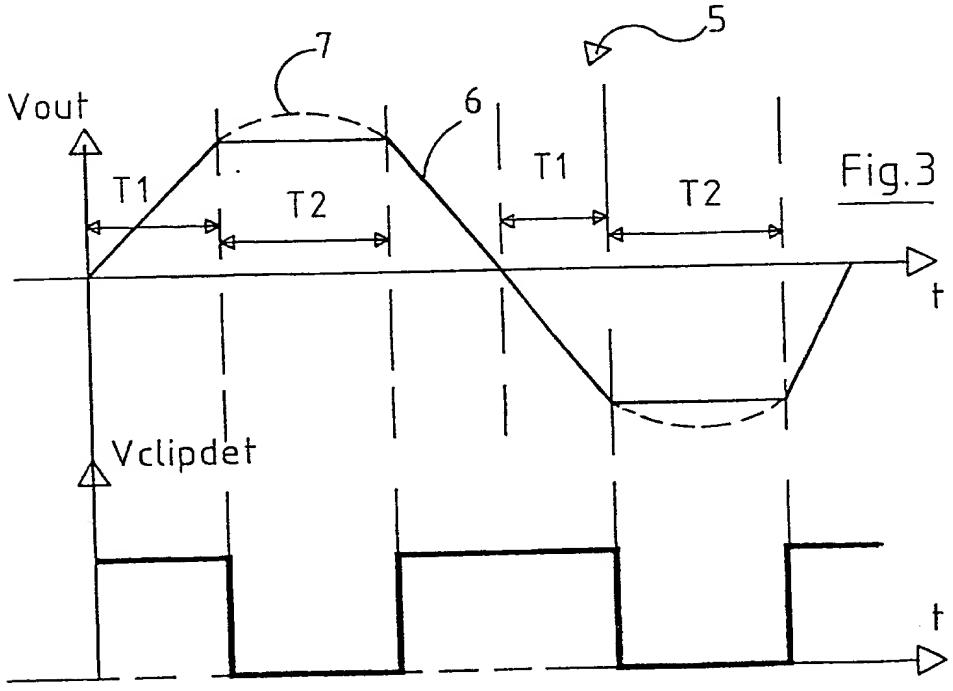

Fig.3

Fig.4

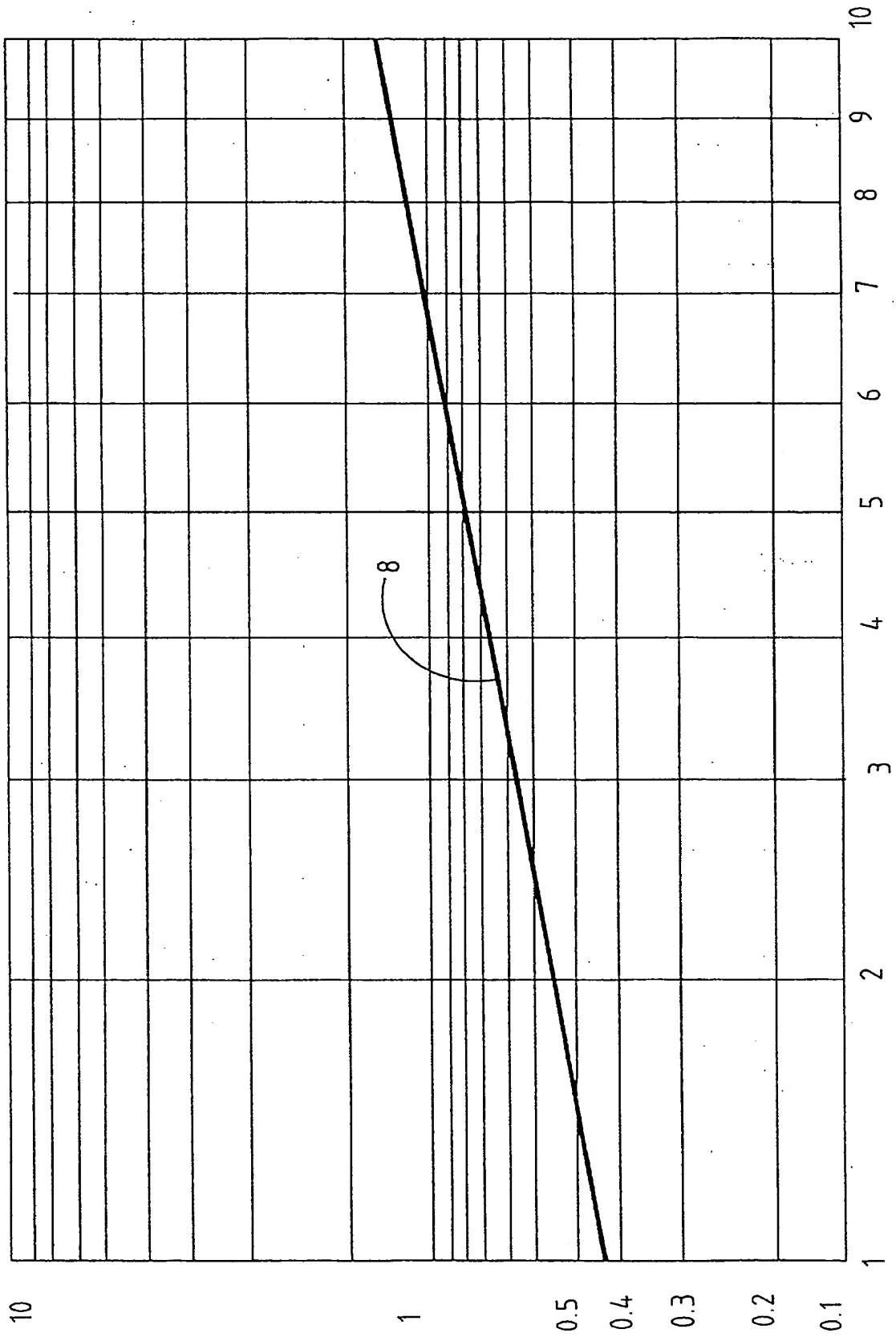

Fig.5

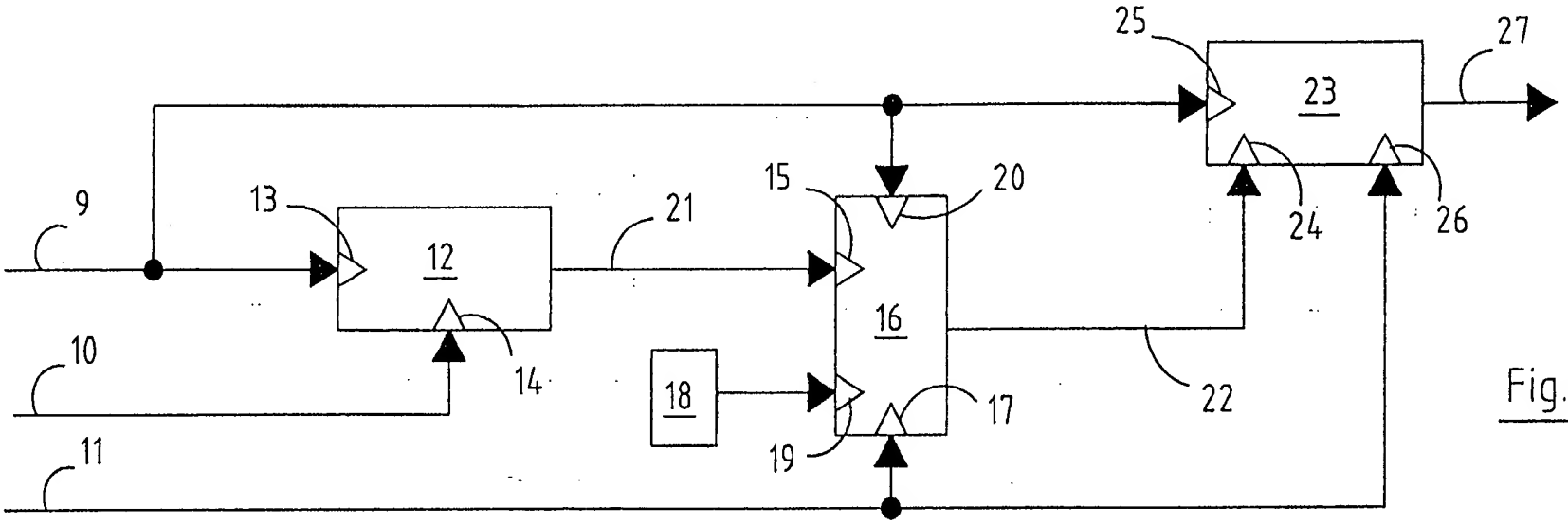

Fig.6

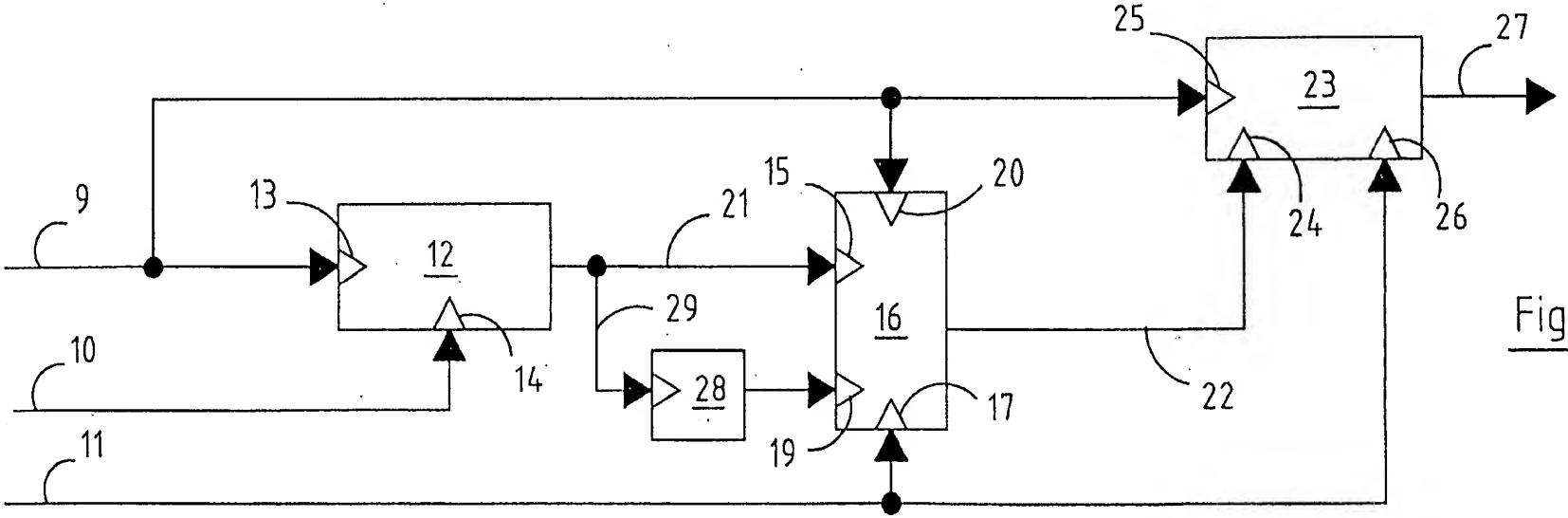

Fig.7

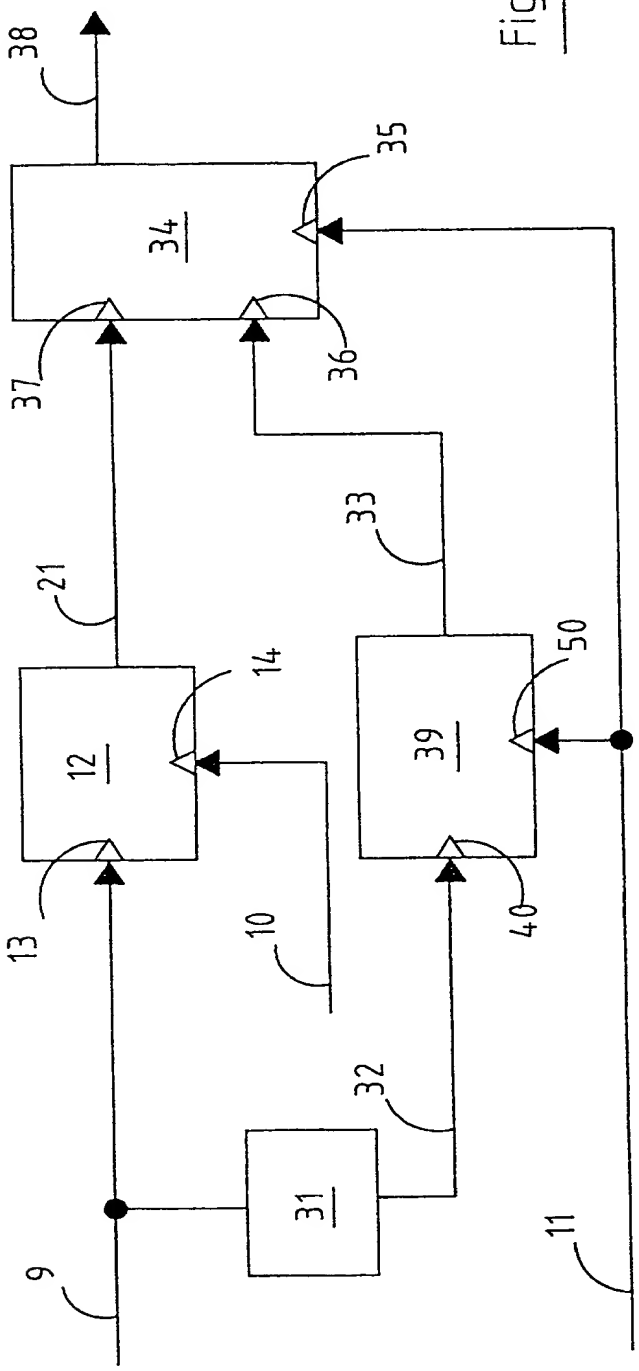
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Fig.8

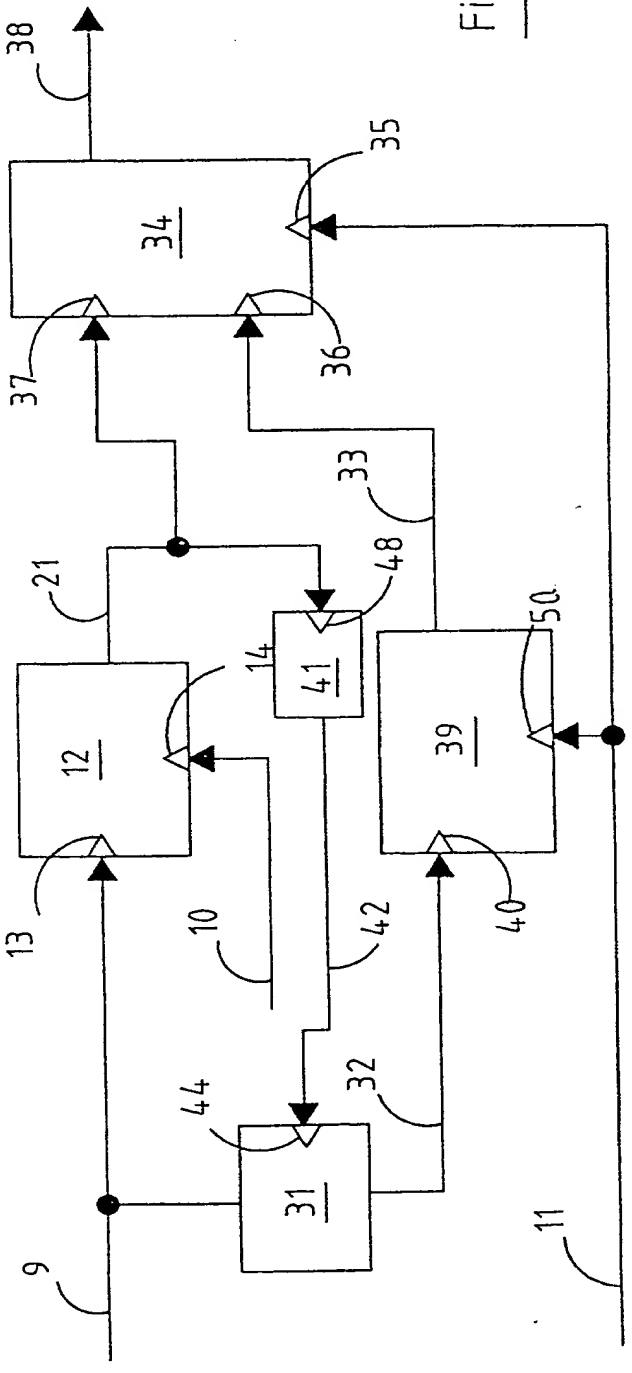
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Fig.9